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PCI Express 3.0 and 4.0 Test Challenges: Link Equalization Testing 8Gbps vs 16Gbps Rx Testing

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BY
NeuHelium

Agenda

PCI-SIG Spec Development: Gen3/Gen4

What is Dynamic Link Equalization

PCI Express PHY Test Requirements (Link EQ)

Rx Jitter Calibration

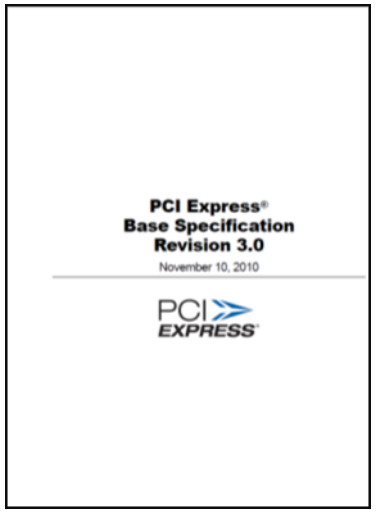
Live Demo of PCIE Link EQ Test

PCIE Gen4 Test Challenges

What We Didn’ t Talk about

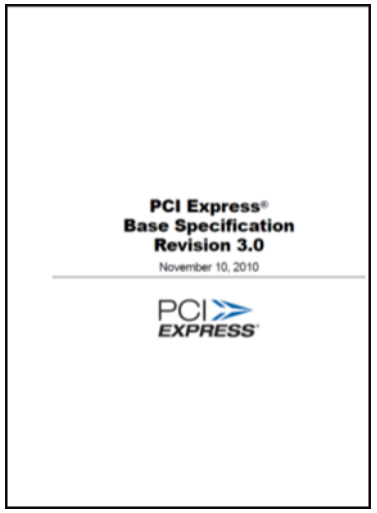
Summary

Sequential Development of PCIe Specs and Scope



Base Specification

- Contains all the system knowledge
- Can directly be applied to Chip Test:



Card Electromechanical (CEM) Spec

- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer’s need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

Phy Test Specification

- Defines compliance tests of CEM spec in detail

Differences on PHY-layer between PCIe2 and PCIe3

	PCIe2	PCIe3
transfer rate	5GT/s	8GT/s
coding	8B/10B	128B/130B
overhead	25%	1.5625%
serial alignment	K-28.5 symbol with CID=5	01b or 10b every 128 bits (transition every 130 bits)
limited CID	code guarantees CID ≤ 5	scrambling with PRBS23 achieves CID ≤ 23
DC-balance	concept of running disparity gurantees DC-balance	scrambling with PRBS23 achieves DC-balance after ~1ms (8Mb)
scrambling	optional	control: no (partially), data: always
data rate / lane	4Gb/s	7.88Gb/s
RX-test	**informative**	**normative**

PCIe 4.0 Outlook and Test Challenges

- New data rate will be added 16GT/s
  - Requires an output stages capable of providing pre-shoot and de-emphasis with fast enough rise-times.
- Link Equalization protocol will be similar
  - TxEQ P0-P10
  - RxEQ CTLE + 2tap DFE
  - Max Channel Length (shorter) – more needs for Re-timers and Re-drivers
- RX clocking architectures: CC, DC and IR
  - CC ➔ Common RefClock ➔ synchronous RX and TX
  - DC ➔ Data Clocked ➔ synchronous or asynchronous RX and TX
  - IR ➔ Independent RefClock ➔ asynchronous RX and TX
  - SKP OS filtering is required!
- RX testing procedure will be standardized for all data rates 2.5GT/s, 5GT/s, 8GT/s and 16GT/s

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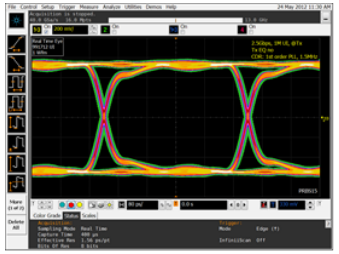
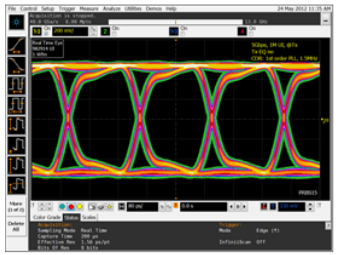
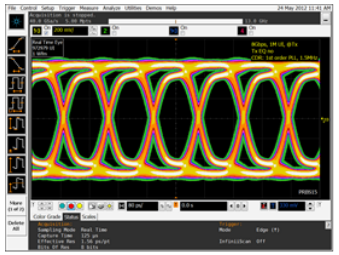
Why Test Receivers





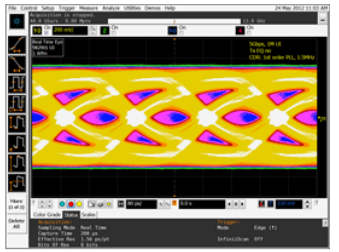


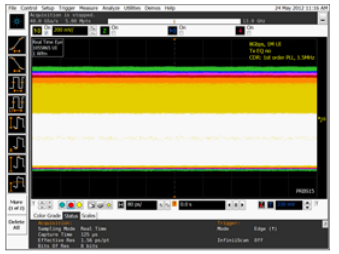
2.5Gbps

5Gbps

8Gbps

16 Gbps





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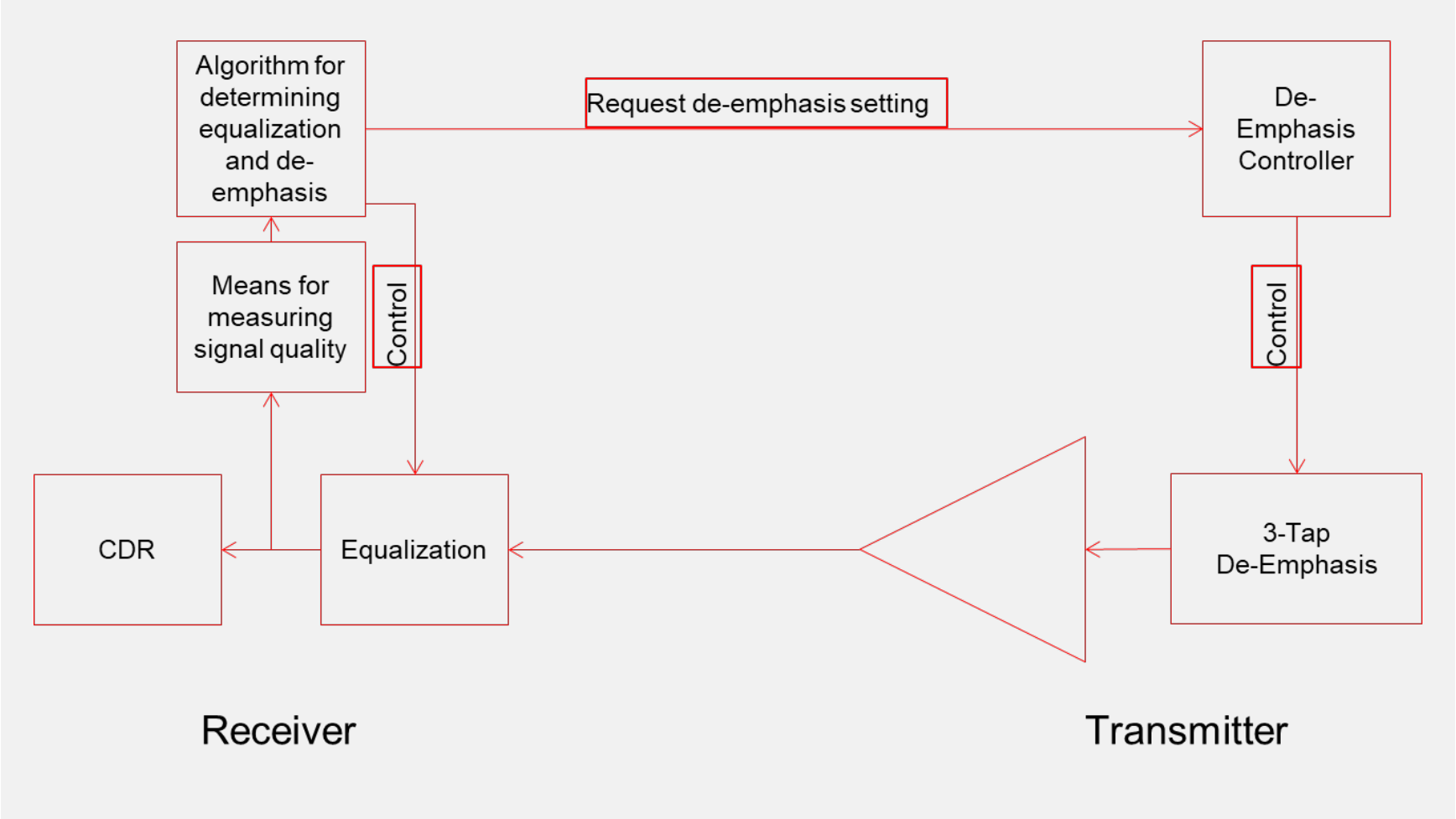
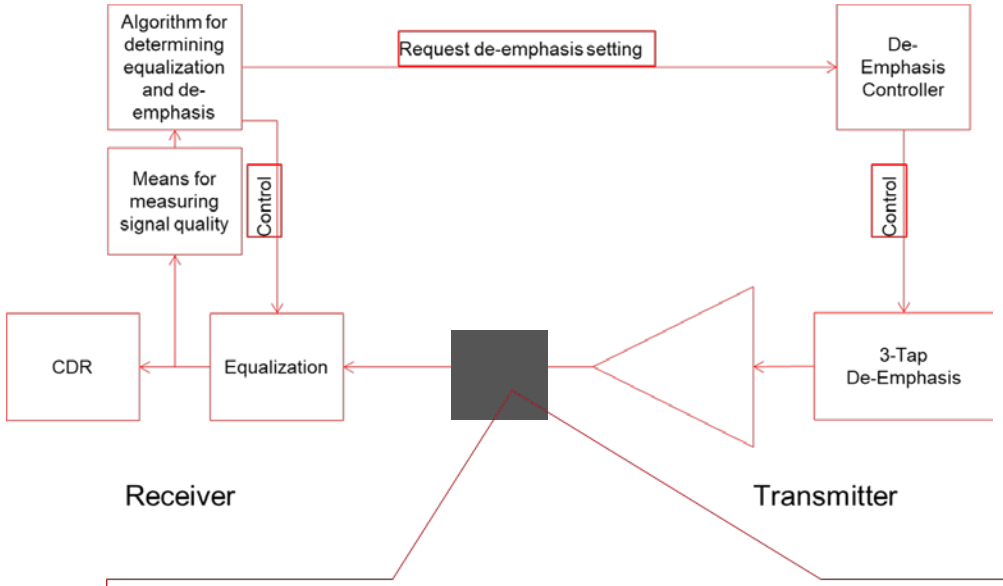
Tx/Rx Link for PCIe 3.0

Block diagram of transmitter and receiver architecture



Dynamic Channel



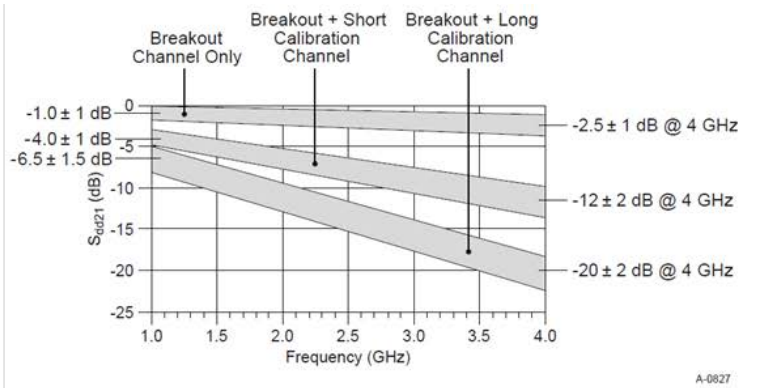
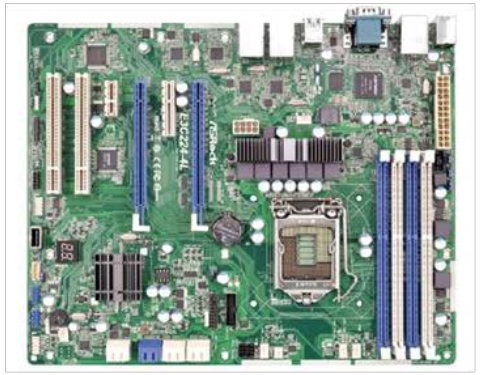
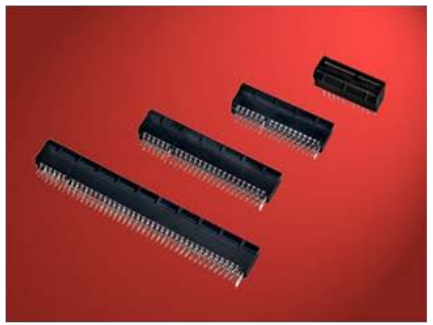


Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels





TxEQ vs RxEQ

RxEQ - CTLE

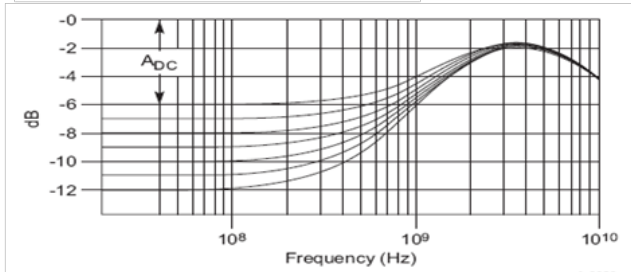


Figure 4-69: Loss Curves for Behavioral CTLE

RxEQ – DFE

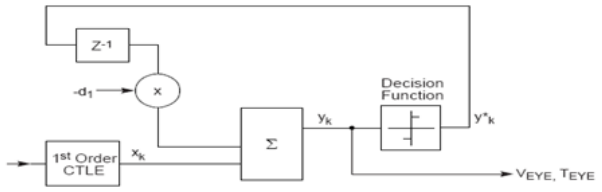
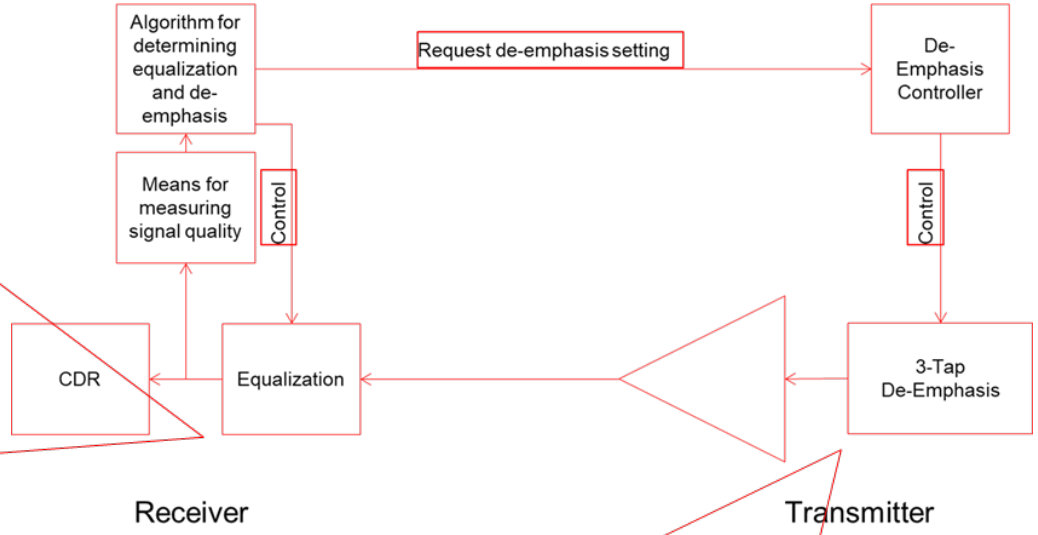
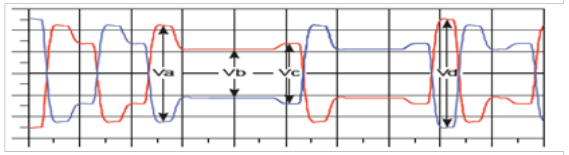


Figure 4-70: Equation and Flow Diagram for 1-tap DFE



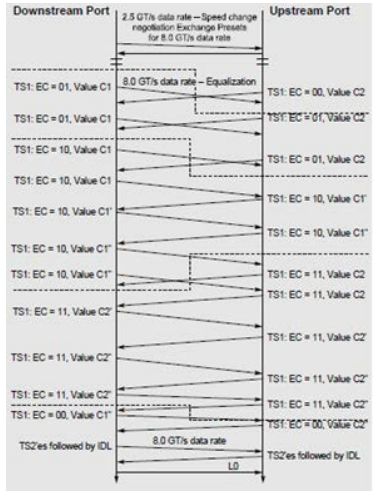
TxEQ – De-emphasis and Pre-shoot

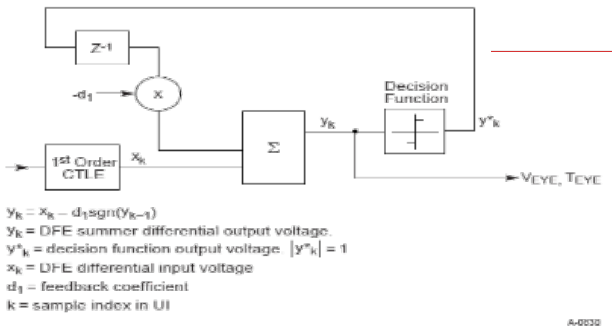


Preset Number	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	See Note 2.

Dynamic Equalization

Root complex and end point will negotiate the optimized eq setting





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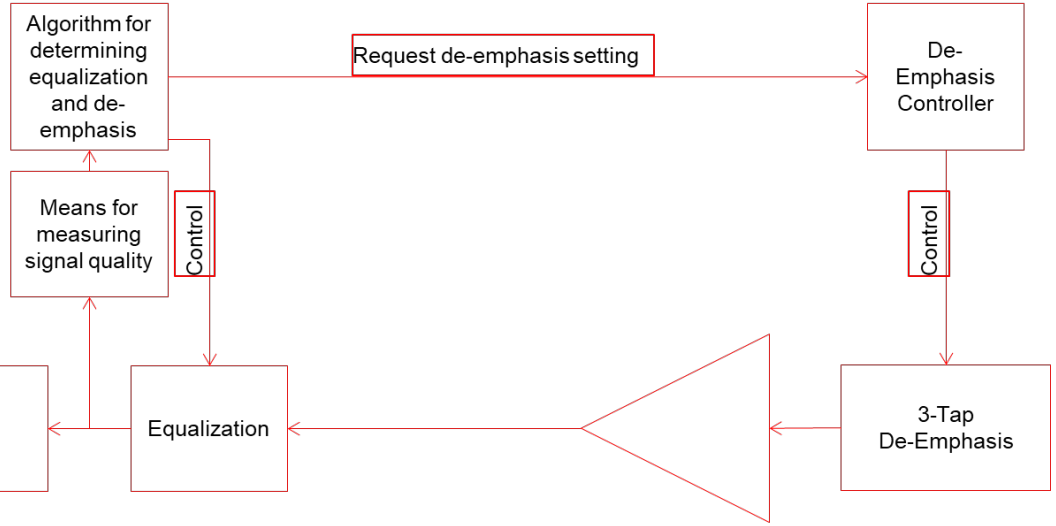

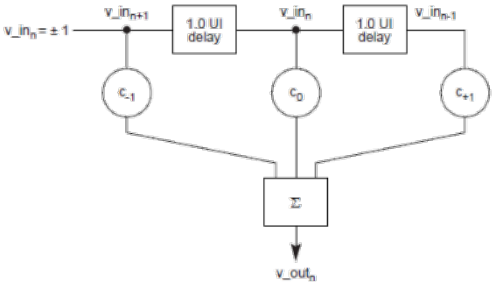

Figure 4-41: Tx Equalization FIR Representation

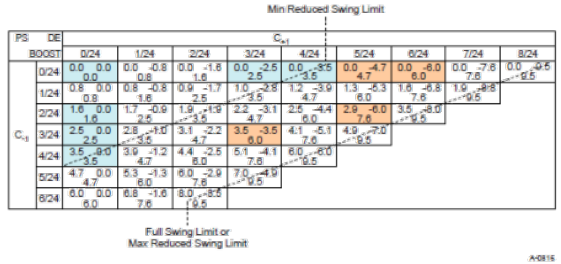

Figure 4-45: TxEQ Coefficient Space Triangular Matrix Example

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Dynamic Link Equalization Handshake

The four phases of the link equalization protocol

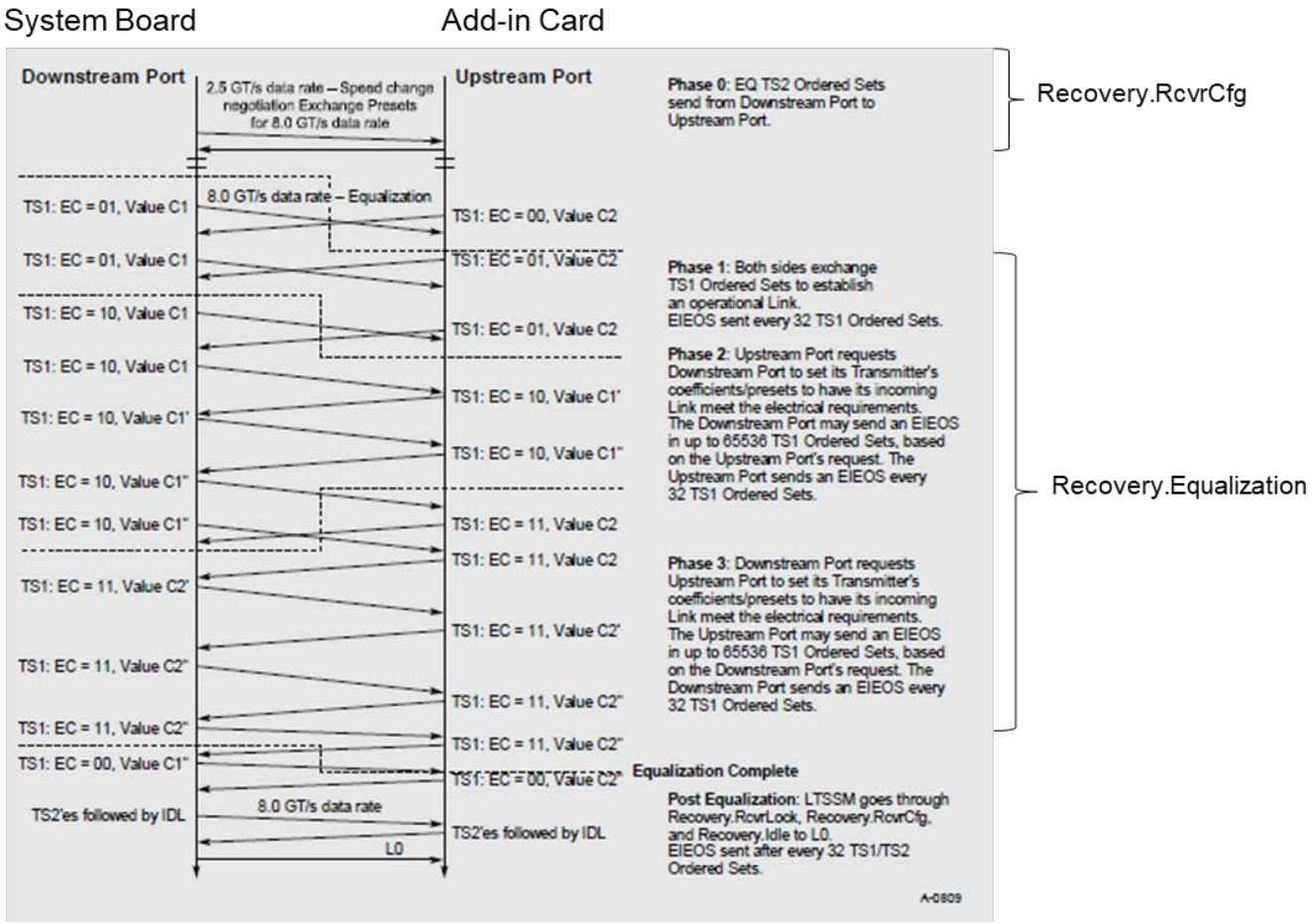
System Board tells the Add-in Card which initial preset to use after the speed change will have been done.

Link partners settle on 8GT/s speed.

Exchange FS/LF values.

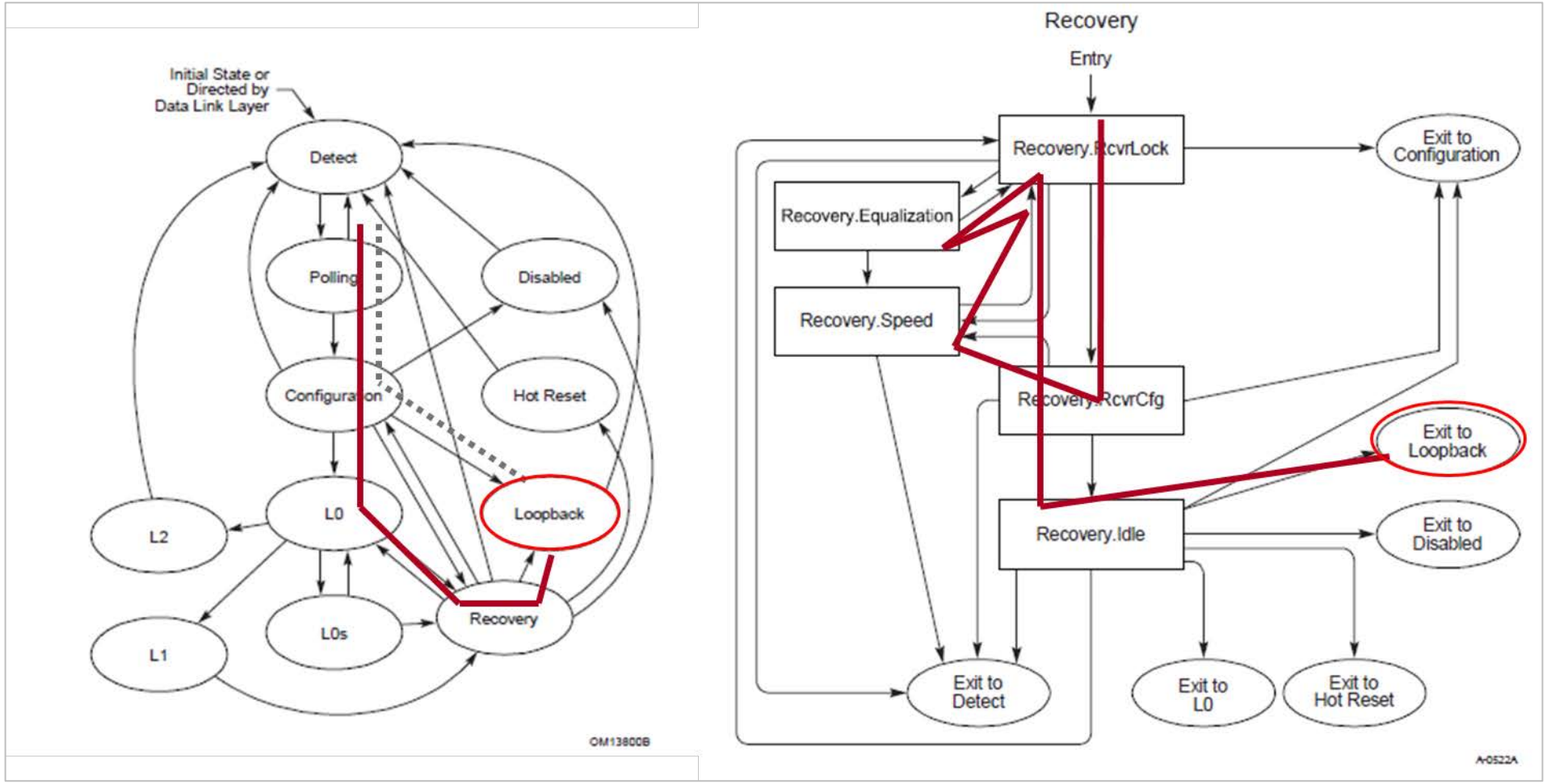
Add-in Card sets up the de-emphasis of the System Board’ s transmitter.

System Board sets up the de-emphasis of the Add-in Card’ s transmitter.



Dynamic Link Equalization Loopback

The link training status state machine



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Live Demo of PCIE Link EQ Test

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What We Didn’ t Talk about

Summary

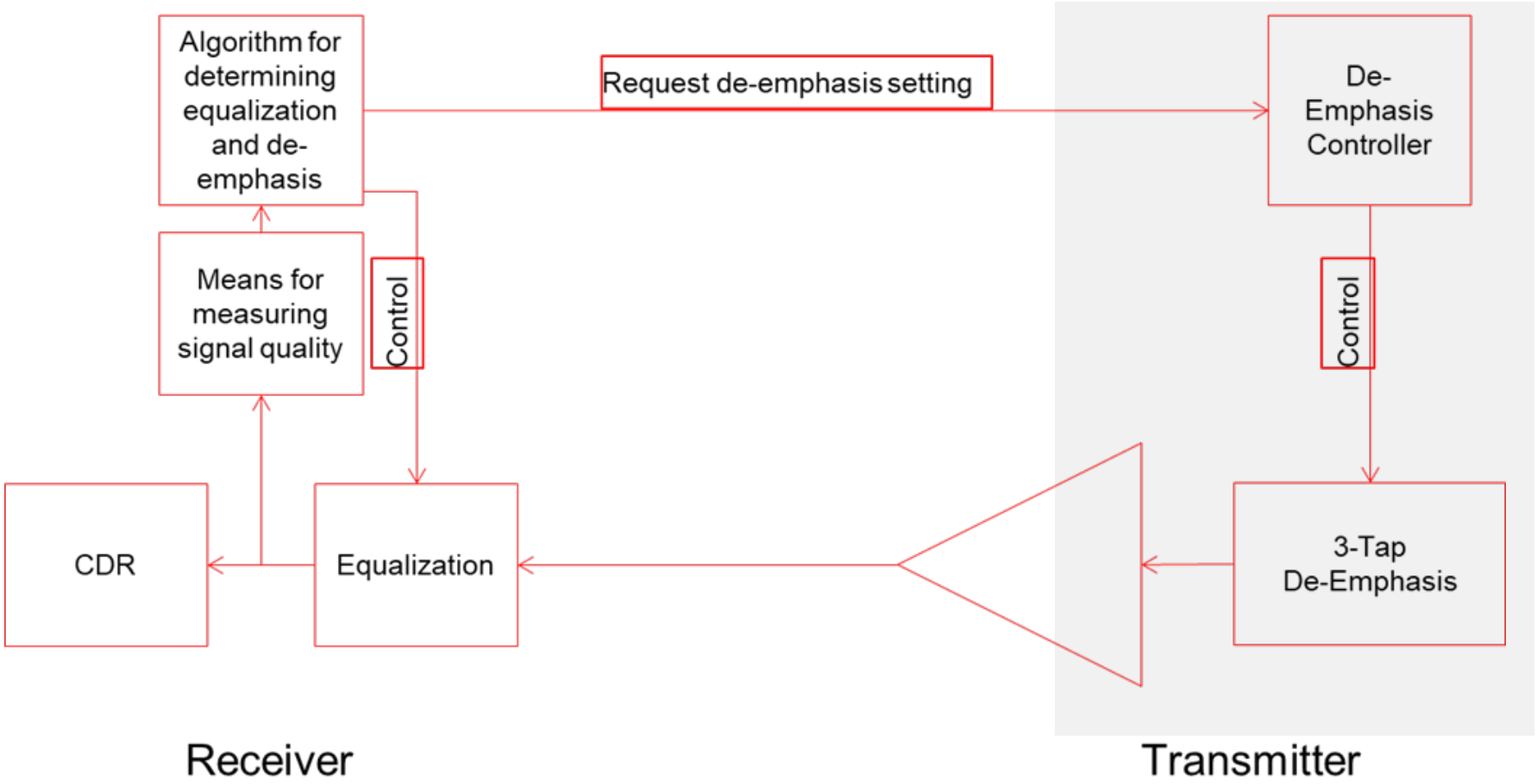
Tx/Rx Link Equalization Testing for PCIe 3.0

According to pci express electrical phy test specification

Test Number	Test Name
2.3	Add-in Card Transmitter Initial Tx EQ Test for 8.0GT/s
2.4	Add-in Card Transmitter Link Equalization Response Test for 8GT/s
2.7	System Board Transmitter Link Equalization Response Test for 8GT/s
2.10	Add-in Card Receiver Link Equalization Test for 8GT/s
2.11	System Board Receiver Link Equalization Test for 8GT/s

Tx/Rx Link Equalization Testing for PCIe 3.0

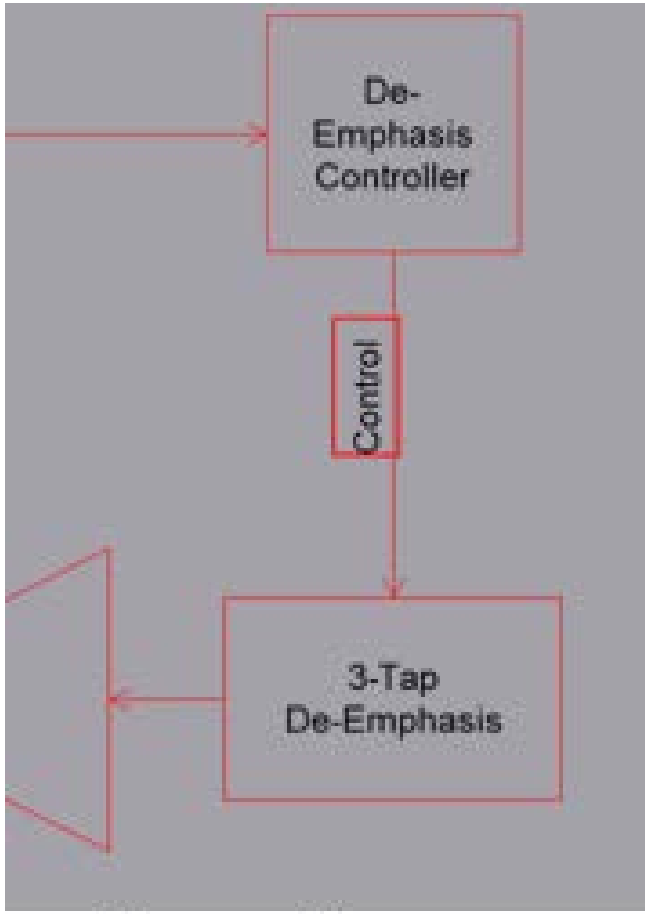
Tests 2.3, 2.4, and 2.7 focus on the transmitter



Tx/Rx Link Equalization Testing for PCIe 3.0

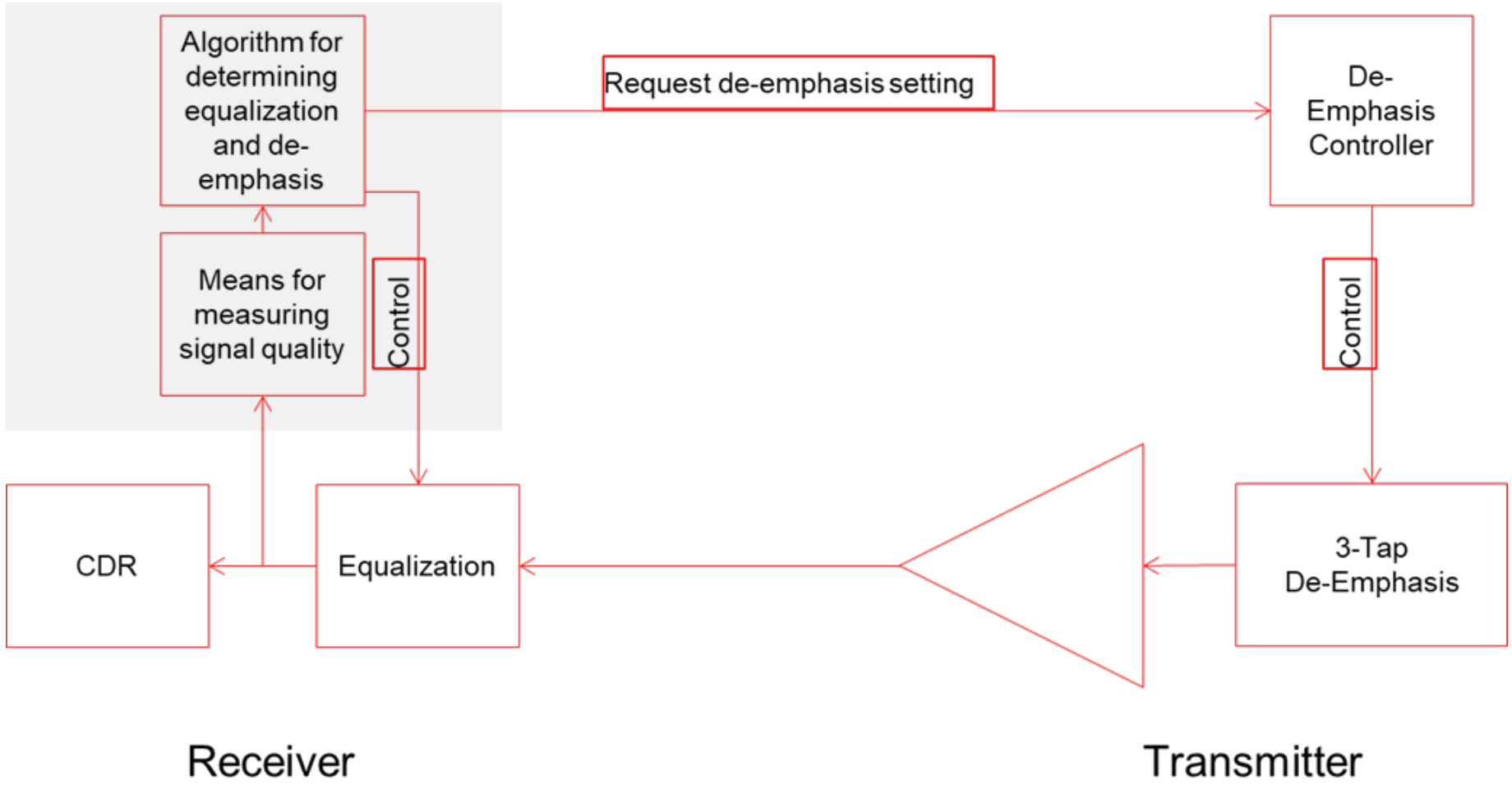
Tests 2.3, 2.4 and 2.7 focus on the transmitter

- The PCIe 3.0 Receiver Link Equalization Tests specified in 2.3 and 2.4 and 2.7 provide insight to TxEQ issues and corner case situations
  - Requires the DUT to negotiate using both Presets and Cursors values
  - Determines if DUT responds to Preset/Cursor requests in the specified amount of time
  - Troubleshoot the issues between protocol communication vs PHY layer performance



Tx/Rx Link Equalization Testing for PCIe 3.0

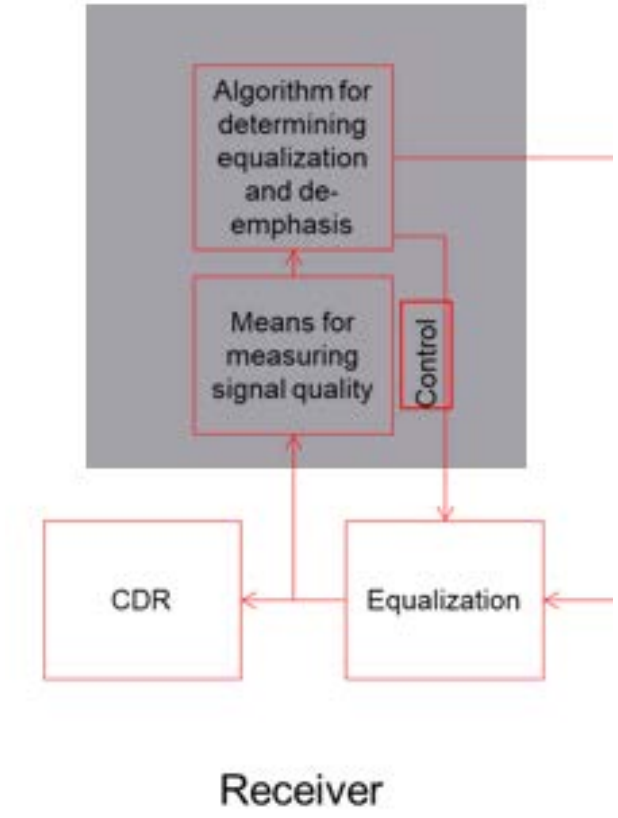
Tests 2.10 and 2.11 focus on the receiver



Tx/Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 and 2.11 focus on the receiver

- The PCIe 3.0 Receiver Link Equalization Tests specified in 2.10 and 2.11 are the most important test of a DUT, they:
  - Determine the DUT’ s ability to request appropriate amounts of transmitter equalization
  - Determine the DUT’ s ability to internally apply the appropriate amount of receiver equalization
  - Determine the quality of the DUT’ s algorithm for optimizing the link quality
  - Determine the DUT’ s ability to optimize TxEQ and RxEQ in a short period of time



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CEM Rx Jitter Tolerance Spec

According to pci express electrical phy test specification

Parameter	Min	Max	Unit	SigTest	
				Technology	Template
Vpp		800	mV	N/A	N/A
RJ (Random Jitter)	1.5	1.7	ps RMS	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
SJ (Sinusoidal Jitter) @ 100 MHz	12.5	13.5	ps PP	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
Differential Mode Sinusoidal Interference at 2.1 GHz	14	16	mV PP	N/A	N/A
$V_{RX-EH-8G}$ Eye Height		AIC: 41 to 46 System: 45 to 50	mV	PCI_3_0_RX_CAL	AIC: PCIE_3_8GB_RX CARD_CAL_MULTI_CTLE_DFE_EMBED01 System: PCIE_3_8GB_RX SYS_CAL_MULTI_CTLE_DFE_ EMBED01
$T_{RX-EW-8G}$ Eye Width		AIC: 39.25 to 41.25 System: 43 to 45	ps	PCI_3_0_RX_CAL	AIC: PCIE_3_8GB_RX CARD_CAL_MULTI_CTLE_DFE_EMBED01 System: PCIE_3_8GB_RX SYS_CAL_MULTI_CTLE_DFE_ EMBED01

Setup

- Build in Jitter Sources:
  - 8 Tap De-emphasis
  - SJ
  - RJ
  - DMI
  - CMI (Base Spec)
  - Clock Multiplier
  - ISI Channel Emulation
  - Error Detector Equalization

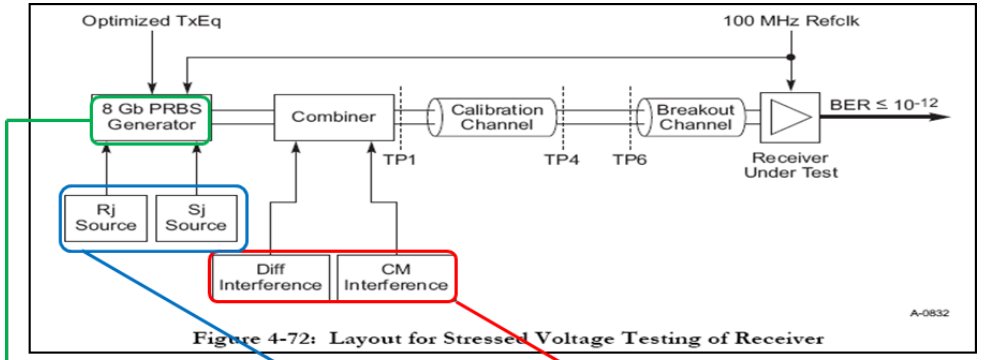
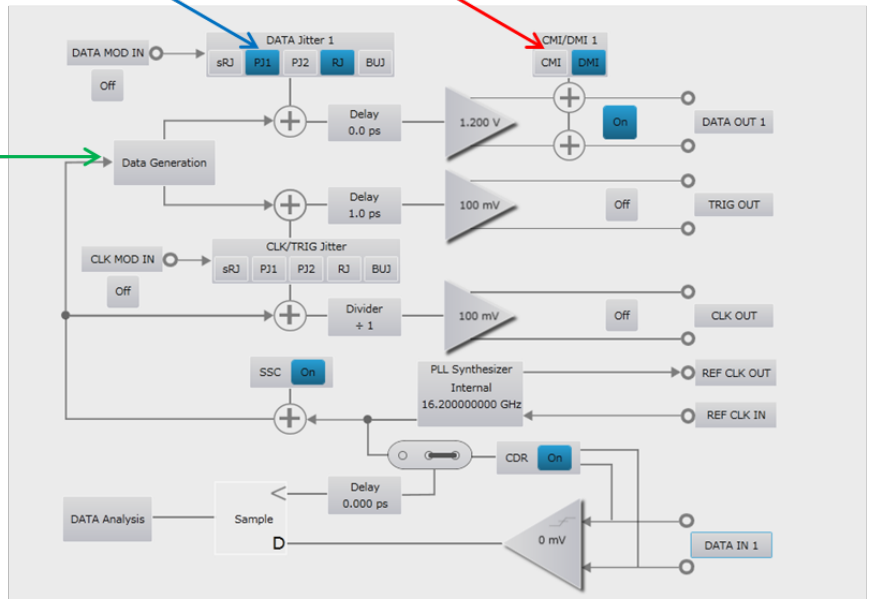
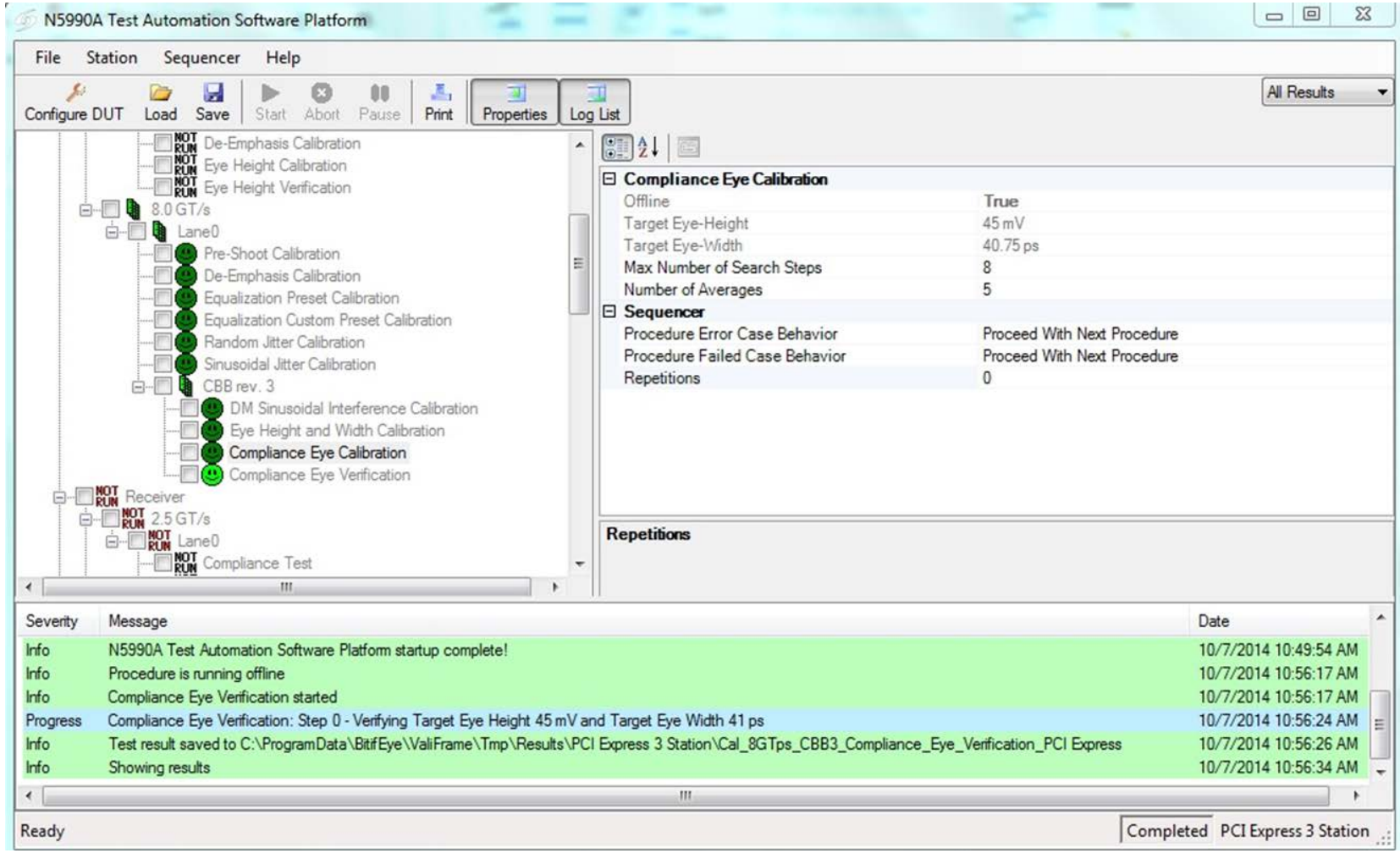


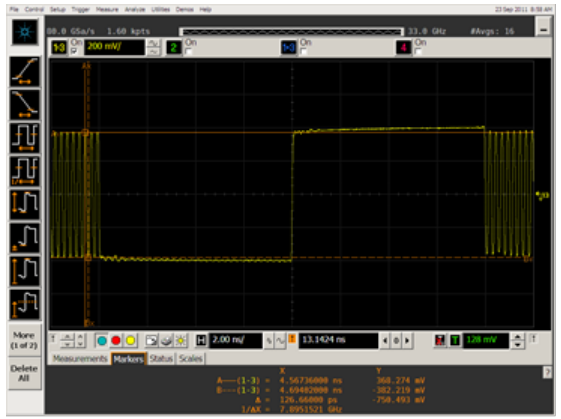
Figure 4-72: Layout for Stressed Voltage Testing of Receiver

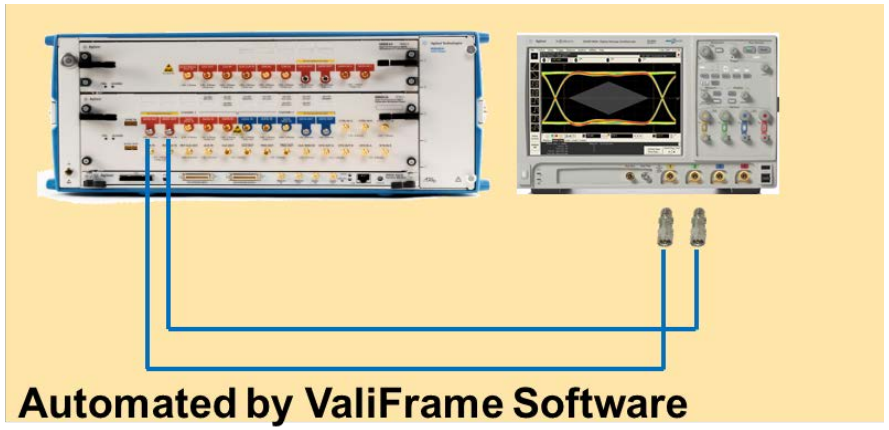


ValiFrame Automation Software



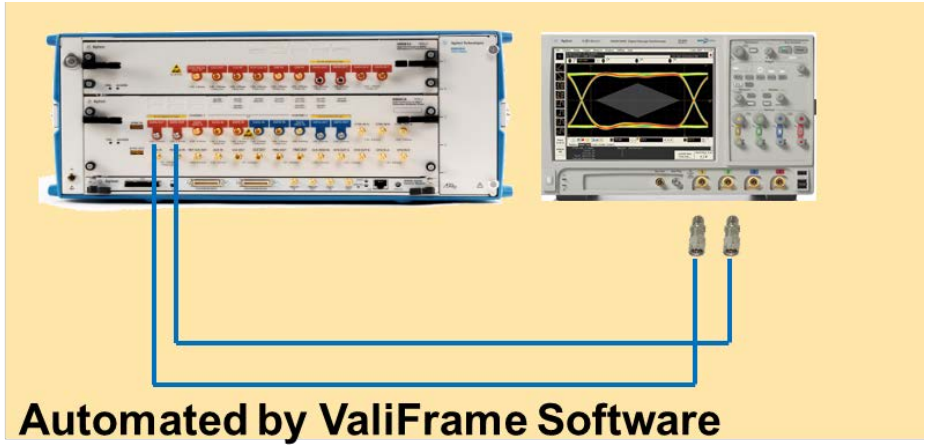
Presets and Amplitude

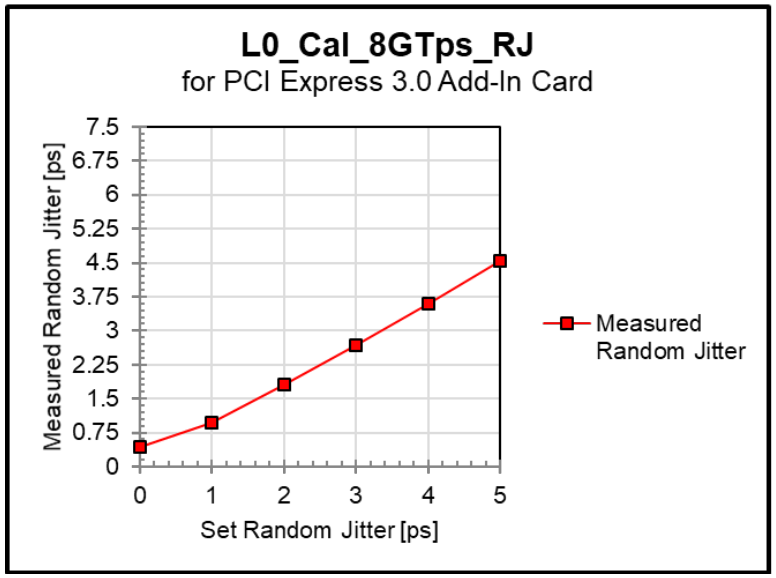


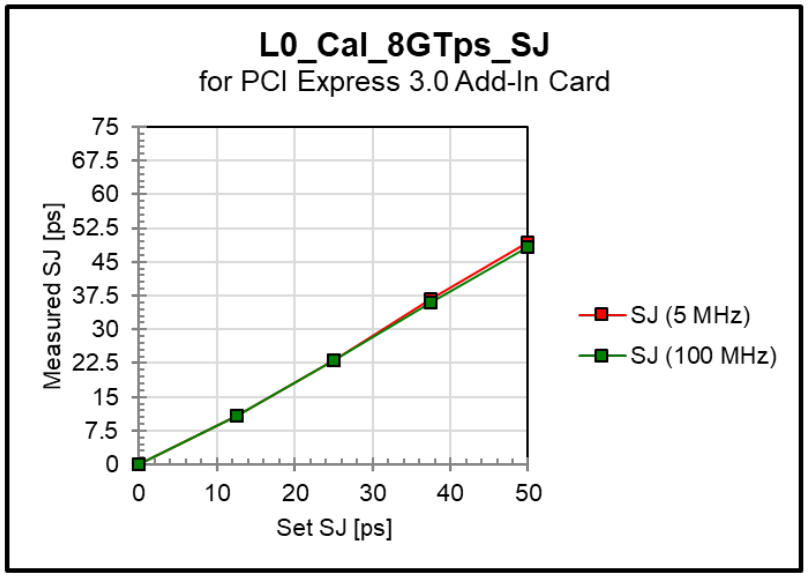


Preset	Pre-Shoot [dB]	De-Emphasis [dB]	Differential Voltage [mV]	Set Pre-Shoot [dB]	Set De-Emphasis [dB]	Set Differential Voltage [mV]
0	0.00	-6.00	800	0.08	-6.02	691
1	0.00	-3.50	800	-0.03	-3.68	681
2	0.00	-4.40	800	0.09	-4.43	676
3	0.00	-2.50	800	0.02	-2.65	681
4	0.00	0.00	800	0.11	-0.32	766
5	1.90	0.00	800	1.92	-0.27	752
6	2.50	0.00	800	2.58	-0.17	755
7	3.50	-6.00	800	3.36	-5.83	681
8	3.50	-3.50	800	3.38	-3.34	664
9	3.50	0.00	800	3.53	-0.09	744

SJ and RJ







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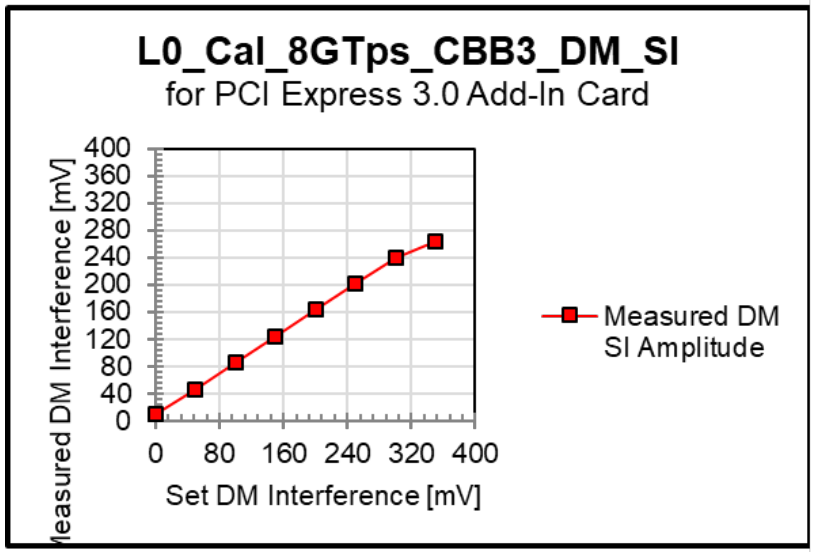
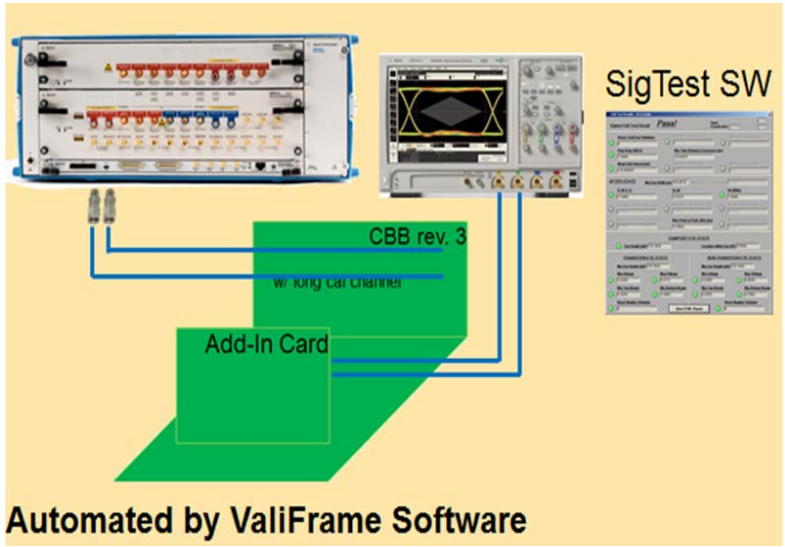
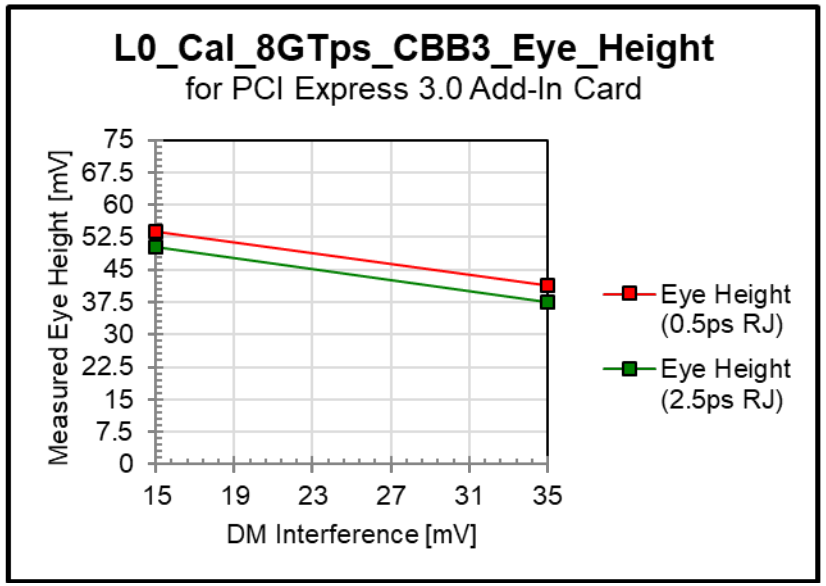
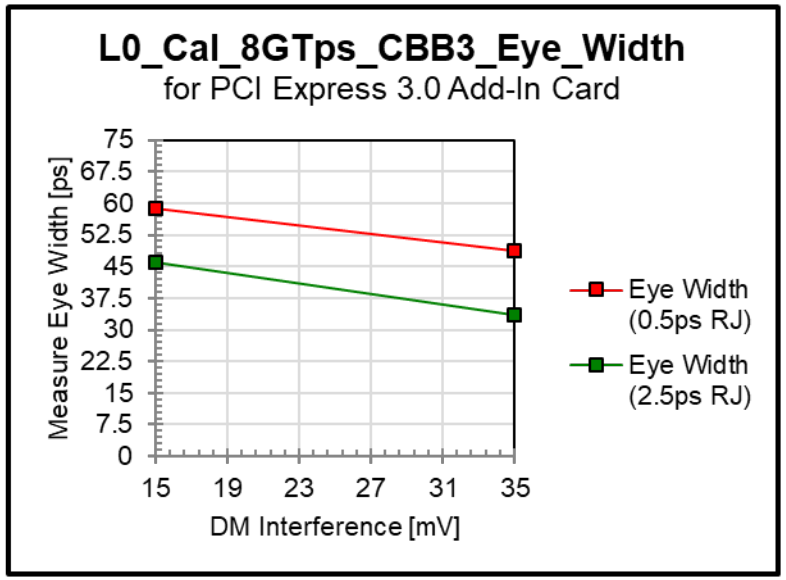
DMI and Eye









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Final Calibrated Eye

Set up BERT to generate compliance pattern with P7 activated:

- Adjust DM-SI to meet specified EH
- Adjust RJ to meet specified EW
- Re-check EH and if necessary re-adjust DM-SI once
- Record the final calibration values RJ_{cal} and $DM\text{-}SI_{cal}$ for later usage

L0_Cal_8GTps_CBB3_Comp_Eye

for PCI Express 3.0 Add-In Card

SigTest Ver	3.1.63
BERT System	DE54300110
Offline	False
Max Number	8
Number of A	5
Scope Conne	ect Connect
Jitter Unit	Time

DMSI [mV]	RJ [ps]	Eye-Height [mV]	Eye-Width [ps]
21.3	2.85	44.8	41.2

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Rx Jitter Calibration

Live Demo of PCIE Link EQ Test

PCIE Gen4 Test Challenges

What We Didn’ t Talk about

Summary

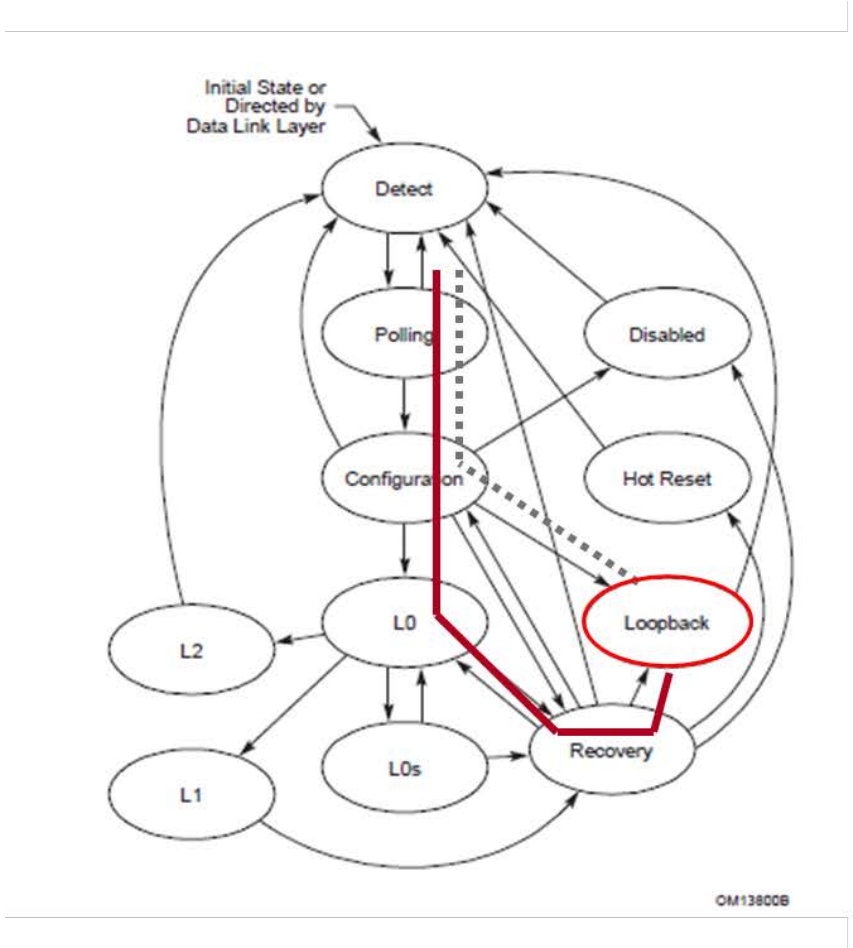
Tx/Rx Link Equalization Testing for PCIe 3.0

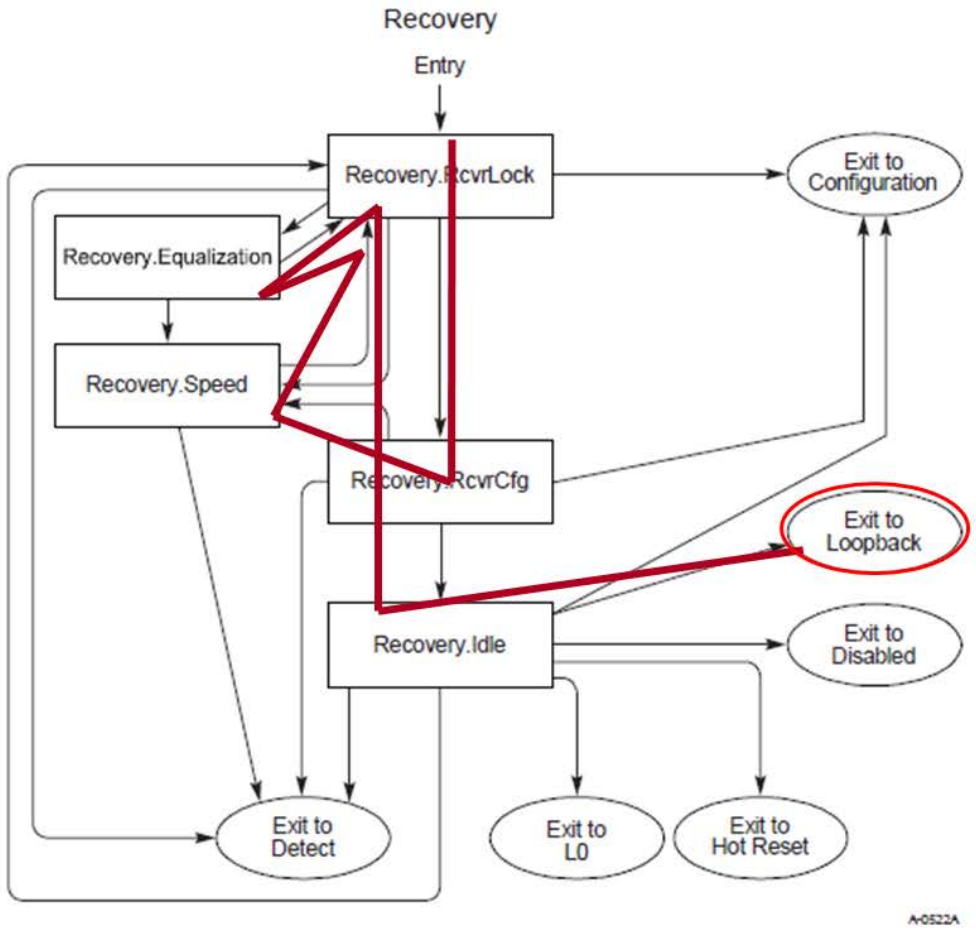
According to pci express electrical phy test specification

Test Number	Test Name
2.3	Add-in Card Transmitter Initial Tx EQ Test for 8.0GT/s
2.4	Add-in Card Transmitter Link Equalization Response Test for 8GT/s
2.7	System Board Transmitter Link Equalization Response Test for 8GT/s
2.10	Add-in Card Receiver Link Equalization Test for 8GT/s
2.11	System Board Receiver Link Equalization Test for 8GT/s

Dynamic Link Equalization Loopback

The link training status state machine





Dynamic Link Equalization Handshake

The four phases of the link equalization protocol

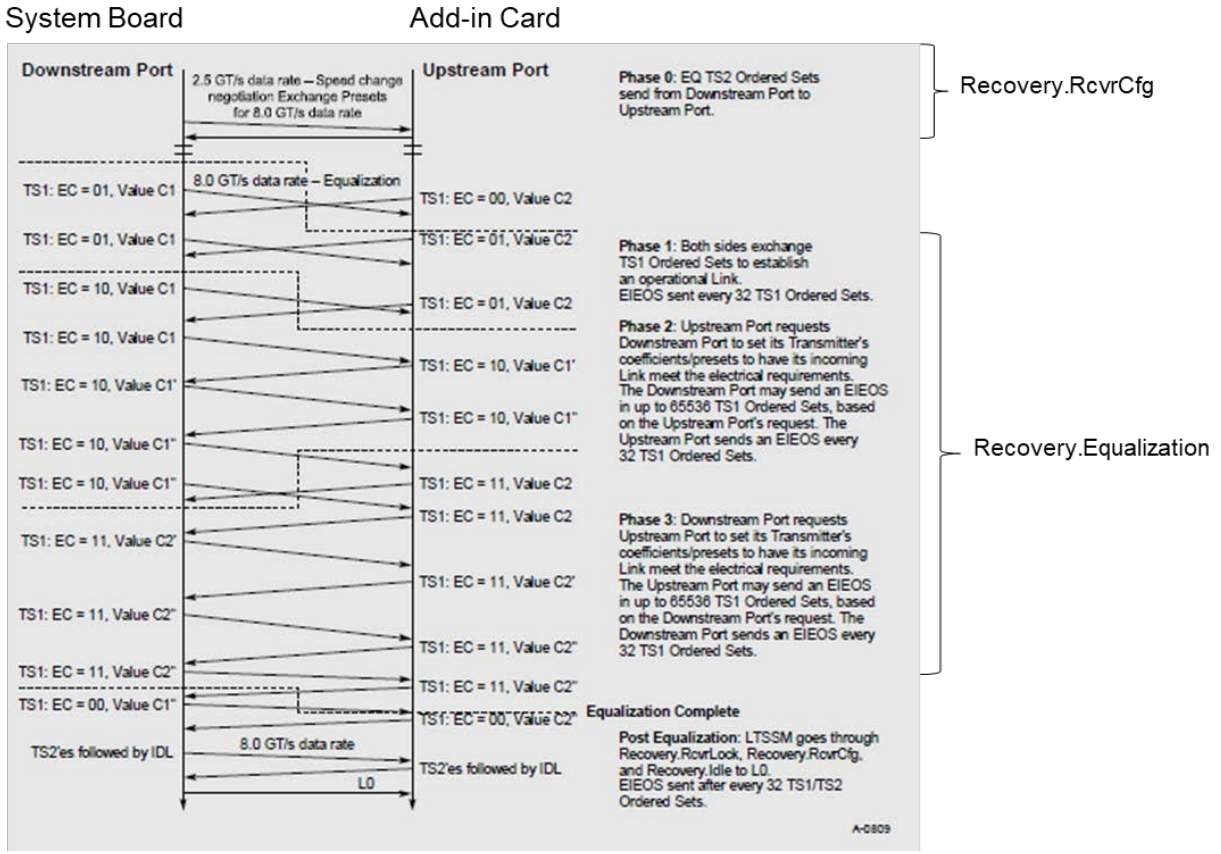
System Board tells the Add-in Card which initial preset to use after the speed change will have been done.

Link partners settle on 8GT/s speed.

Exchange FS/LF values.

Add-in Card sets up the de-emphasis of the System Board’ s transmitter.

System Board sets up the de-emphasis of the Add-in Card’ s transmitter.



M8020A J-BERT LTSSM Capture

Link training logging: ltssm state transitions

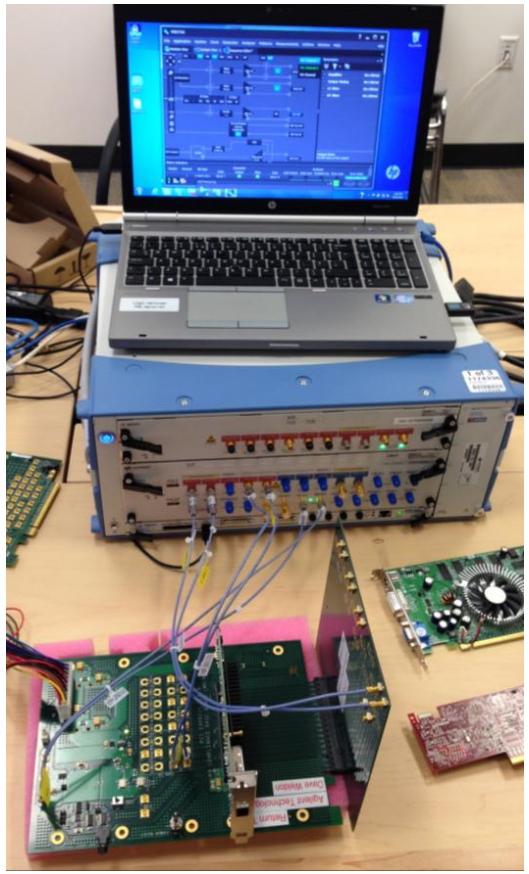
Link Training Logging for M1.DataOut1 at 9/16/2014 9:36:21 AM

Timestamp	State
1.04864 ms	Detect.Active
1.055424 ms	Polling.Active
1.36 us	Polling.Configuration
2.896 us	Configuration.Linkwidth.Start
304 ns	Configuration.Linkwidth.Accept
2.72 us	Configuration.Lanenum.Wait
544 ns	Configuration.Lanenum.Accept
3.568 us	Configuration.Complete
256 ns	Configuration.Idle
224 ns	L0
3.6 us	Recovery.RcvrLock
2.496 us	Recovery.RcvrCfg
8.432 us	Recovery.Speed
448 ns	Recovery.RcvrLock
2.205488 ms	Recovery.Equalization.Phase1
20.867728 ms	Recovery.Equalization.Phase2
1.12 us	Recovery.Equalization.Phase3
1.952 us	Recovery.RcvrLock
672 ns	Recovery.RcvrCfg
112 ns	Recovery.Idle
2.816 us	Loopback.Entry
-	Loopback.Active

PCIe 3.0 Receiver Link Equalization Testing

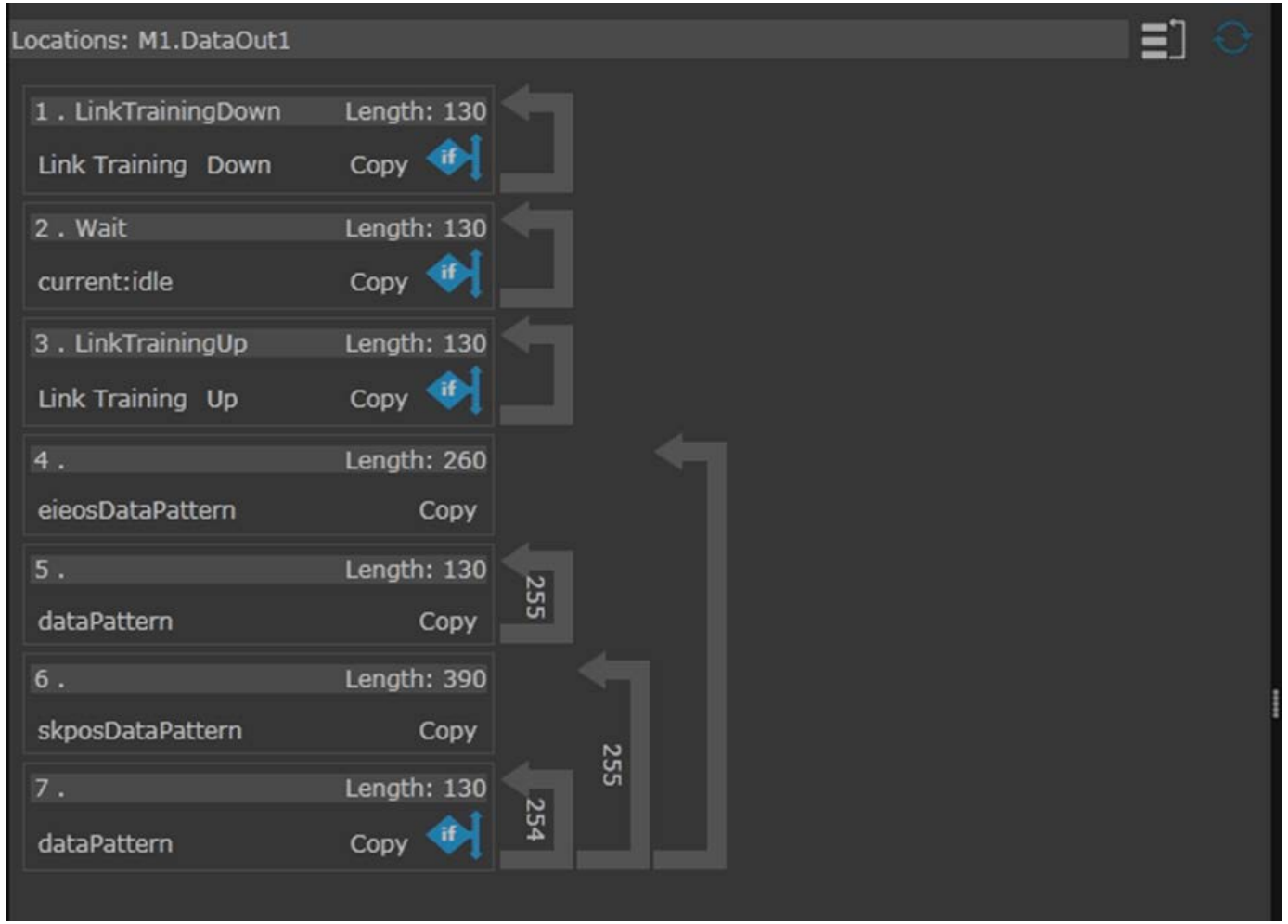
Example of aic tests

- Measurements made with M8020A J-BERT and PCI-SIG interface boards
  - Full calibrations were performed
  - Integrated de-emphasis and sinusoidal interference give us a very clean lab bench (ignore all the mess in the background, it’ s not necessary for the test!)



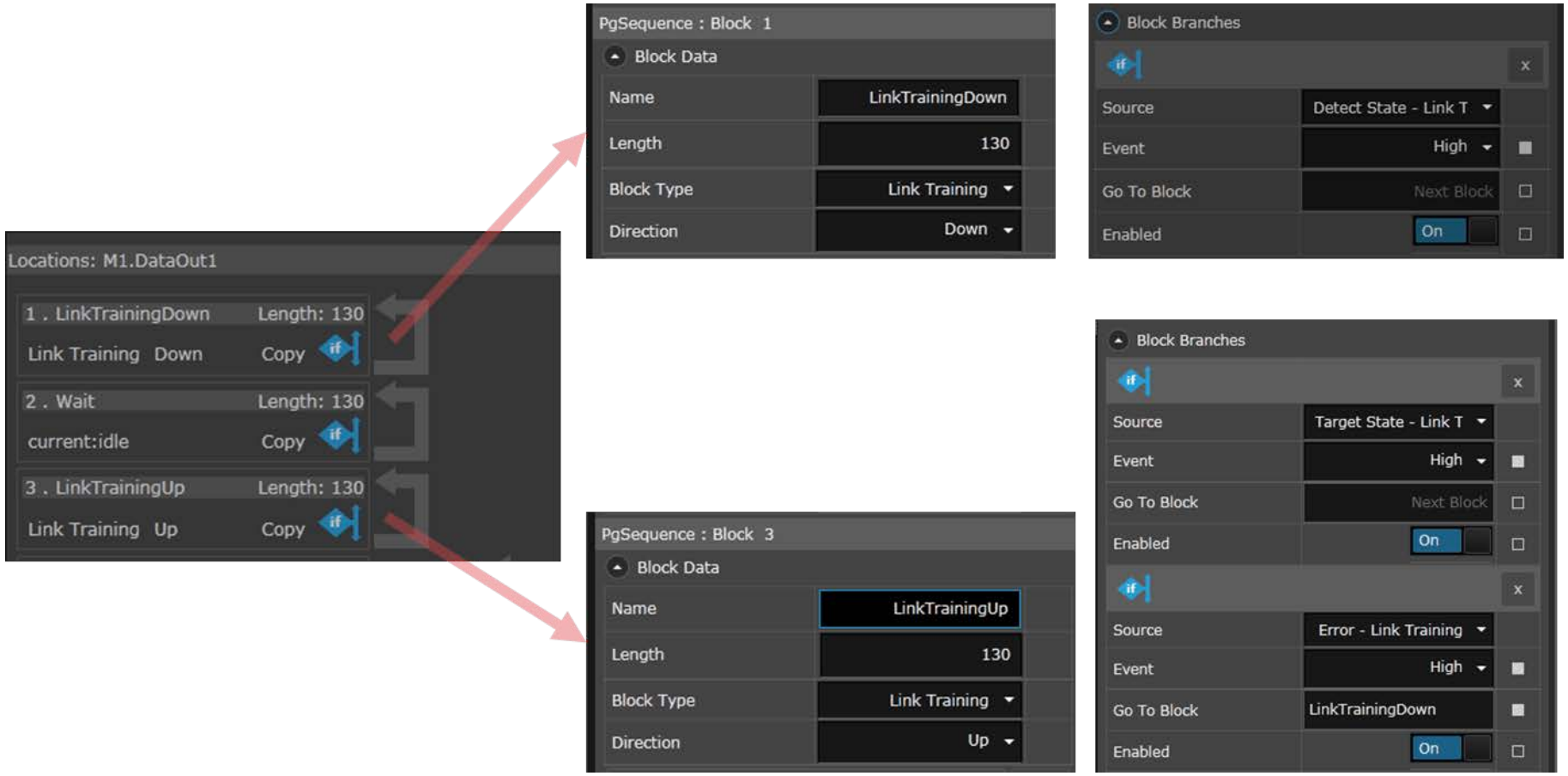
M8020A J-BERT PCIe 3.0 Link Training

Logic-enabled sequencer



M8020A J-BERT PCIe 3.0 Link Training

Protocol-enabled link training sequence blocks



M8020A J-BERT PCIe 3.0 Link Training

Link training logging: link equalization settings

Accept	PresetNumber	PreCursor	DataCursor	PostCursor
True	P7	-	-	-
True	-	0	24	0
True	-	2	22	0
True	-	4	20	0
True	-	6	18	0
True	-	6	16	2
True	-	4	18	2
True	-	2	20	2
True	-	0	22	2
True	-	0	20	4
True	-	2	18	4
True	-	4	16	4
True	-	2	16	6
True	-	0	18	6
True	-	0	16	8
True	-	1	22	1
True	-	3	20	1
True	-	5	18	1
True	-	5	16	3
True	-	3	18	3
True	-	1	20	3
True	-	1	18	5
True	-	3	16	5
True	-	1	16	7
True	-	0	24	0

Different DUT LTSSM Examples

Link training logging: link equalization settings

Accept	PresetNumber	PreCursor	DataCursor	PostCursor
True	P7	-	-	-
True	-	0	24	0
True	-	0	23	1
True	-	0	22	2
True	-	0	21	3
True	-	0	20	4
True	-	0	19	5
True	-	0	18	6
True	-	0	17	7
True	-	0	16	8
True	-	1	23	0
True	-	1	22	1
True	-	1	21	2
True	-	1	20	3
True	-	1	19	4
True	-	1	18	5
True	-	1	17	6
True	-	1	16	7
True	-	2	22	0
True	-	2	21	1
True	-	2	20	2
True	-	2	19	3
True	-	2	18	4
True	-	2	17	5
True	-	2	16	6

Different DUT LTSSM Examples

Link training logging: link equalization settings

Accept	PresetNumber	PreCursor	DataCursor	PostCursor
True	-	3	21	0
True	-	3	20	1
True	-	3	19	2
True	-	3	18	3
True	-	3	17	4
True	-	3	16	5
True	-	4	20	0
True	-	4	19	1
True	-	4	18	2
True	-	4	17	3
True	-	4	16	4
True	-	5	19	0
True	-	5	18	1
True	-	5	17	2
True	-	5	16	3
True	-	6	18	0
True	-	6	17	1
True	-	6	16	2
True	-	4	17	3

Agenda

PCI-SIG Spec Development: Gen3/Gen4

What is Dynamic Link Equalization

PCI Express PHY Test Requirements (Link EQ)

Rx Jitter Calibration

Live Demo of PCIE Link EQ Test

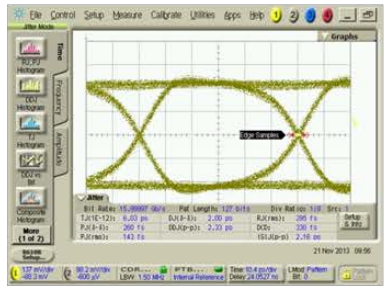
PCIE Gen4 Test Challenges

What We Didn’t Talk about

Summary

Integration at 16Gbps

>16Gbps BERT



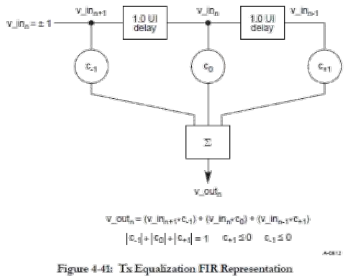
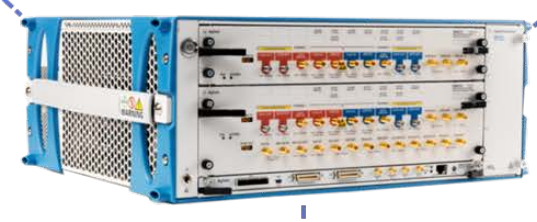


Figure 4-41: Tx Equalization FIR Representation



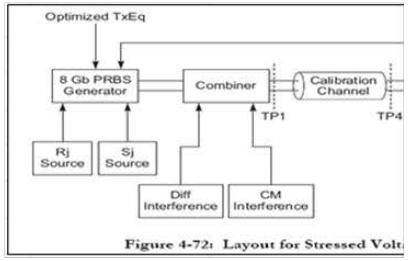
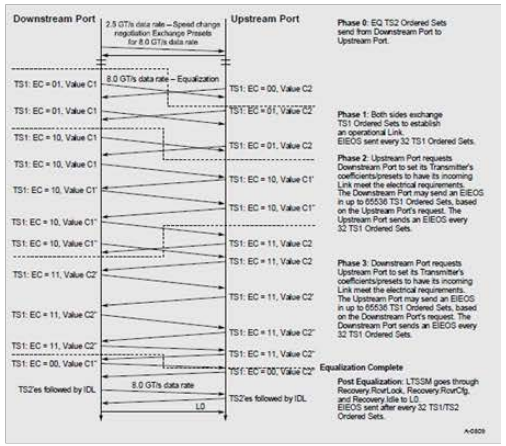


Figure 4-72: Layout for Stressed Volt

Jitter and De-emphasis

Link Equalization



New Test Challenges:

ISI Channel Emulation

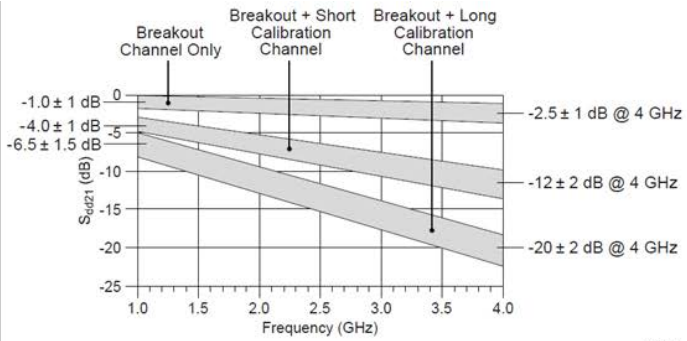
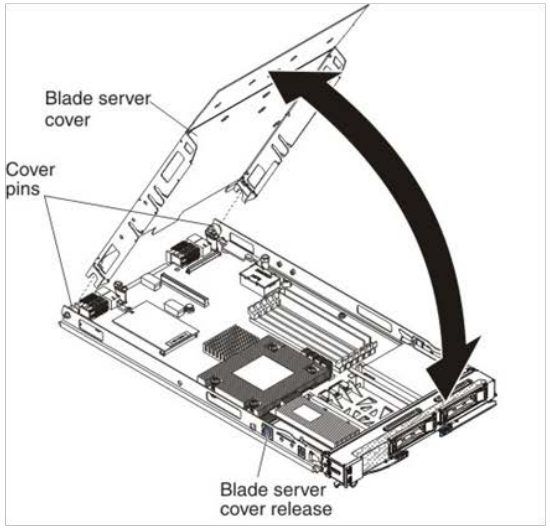


Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels



Error Detector equalization (**CTLE** 16G) to overcome long DUT channels

Agenda

PCI-SIG Spec Development: Gen3/Gen4

What is Dynamic Link Equalization

PCI Express PHY Test Requirements (Link EQ)

Rx Jitter Calibration

Live Demo of PCIE Link EQ Test

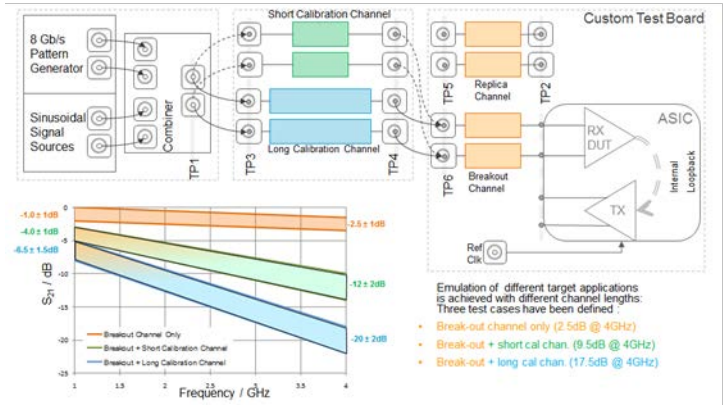
PCIE Gen4 Test Challenges

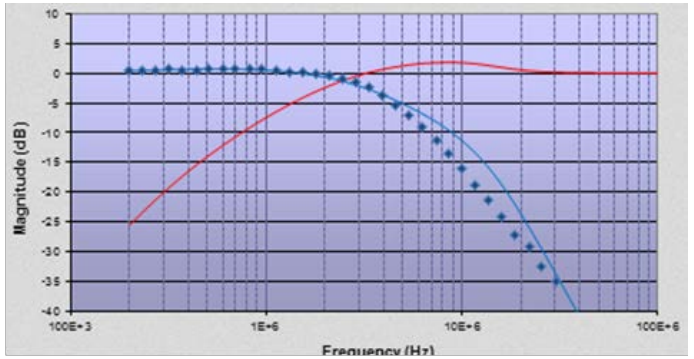
What We Didn’t Talk about

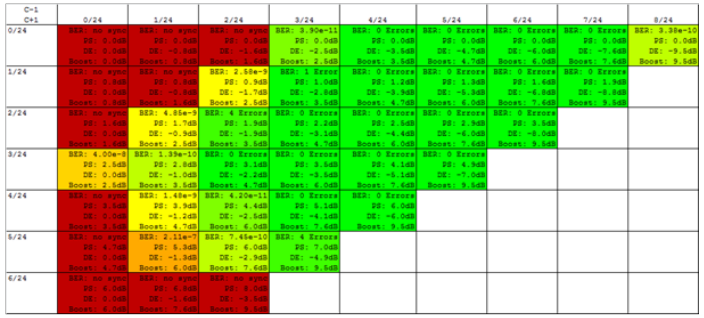
Summary

Other Topics

- Base Spec Testing/Embedded Applications
  - Sigtest vs Seasim
  - Calibration and Test
- Receiver BER Test (BERT functionalities)
  - Loopback through Config
  - Loopback through L0 and Link EQ
- PLL Testing







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Agenda

PCI-SIG Spec Development: Gen3/Gen4

What is Dynamic Link Equalization

PCI Express PHY Test Requirements (Link EQ)

Rx Jitter Calibration

Live Demo of PCIE Link EQ Test

PCIE Gen4 Test Challenges

What We Didn’ t Talk about

Summary

Introducing the Protocol Aware M8020A J-BERT

Take the express lane to design verification

16 / 32Gb/s BERT, 1-4 channels

Highly integrated functionality

- 8-tap de-emphasis
- CDR with adjustable LBW & peaking
- PLL clock multiplication with adjustable LBW
- CTLE analyzer equalization
- Common- and Differential-Mode Sinusoidal Interference (CMSI/DMSI)

Protocol awareness

- On-the-fly encoding and decoding (8b/10b, 128b/130b, 128b/132b)
- Scrambler reset, seed, and start sequencing
- Symbol Error Ratio (SER) and Frame Error Ratio (FER) measurements
- Skip Order Set (SKPOS) addition/subtraction for asynchronous clocks
- Dynamic Link Equalization negotiation
- Analysis of Link Training Status State Machine (LTSSM) state transitions


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